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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/728,193	11/30/2000	Etsuo Morita	09792909-4714	4426

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EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1722	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/728,193	MORITA, ETSUO	
	Examiner	Art Unit	
	Matthew J. Song	1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-20 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-20 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/30/2005 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4-20 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pribat et al (US 4,952,526) or Tsuda et al (US 6,294,440) in view of Natsume (US 5,672,520).

Pribat et al discloses a wafer **1** made of GaAs or InP (claim 14), this reads on applicant's basal body, depositing a dielectric thin layer **2** of silicon nitride, this reads on applicant's nitride pattern, or silica (claim 12-13), where excellent deposition selectivity can be obtained between GaAs and a silicon nitride film by plasma assisted CVD (claim 16-17) (col 10, ln 1-35) with a thickness between $5x10^{-2}$ and a few micrometers, etching a set of bands **23,24** (claim 2 and 7) on the dielectric using means known to those skilled in the art such as photolithography or wet or

dry chemical attack (col 4, ln 50-60), where the bands **23,24** have a width of 0.5 to a few microns and being spaced out at distances of some microns to several hundred microns, thus periodically baring the substrate (col 10, ln 50-67 and col 11, ln 1-10 and Figs 23-24). Pribat et al also discloses a deposition of a thin film of III-V compound is deposited on the preceding structure by MOCVD, with a thickness of a few hundred angstroms to a few microns and depositing a second layer of dielectric, with a thickness of a few hundred angstroms to a few micrometers (col 11, ln 11-38 and Fig 26). Pribat et al also discloses apertures are etched in a second layer of the dielectric and the apertures are offset with respect to the previous ones and the offset can vary from some micrometers to some hundreds of micrometers, this reads on applicant's forming patterns at least partly overlie one another and at least partly do not overlie one another. Pribat et al also discloses III-V polycrystalline material is removed by chemical attack through the apertures, this reads on applicant's forming an indentation (claim 16-19) so as to bare the monocrystalline seed through the apertures and growing a thin layer of monocrystalline III-V material between the dielectric layers and the upper dielectric is removed throughout the surface of the wafer so as to obtain a monocrystalline thin layer of semiconductor (claim 17) (col 11, ln 39-67 and Fig 27). Pribat et al also discloses repeating the disclosed method to obtain a stacking shown in Fig 14 (claims 16-19) (col 12, ln 1-25 and Figs 22-31). Pribat et al discloses a base layer **32** in Fig 31 (claims 11 and 16-19). Pribat et al also discloses a first pattern of dielectric material **50** and **51** with different lengths than a second pattern of dielectric material **20** and **21** in Fig 19.

Tsuda et al discloses a GaN layer **101**, this reads on applicant's base layer, is grown to a thickness of about 4 micrometers on a sapphire substrate **100** (claim 14) is placed in a growth

chamber and a first patterned mask made of SiO_2 (claim 12-13) is formed on the GaN layer **101** by sputtering (claim 15) and the SiO_2 film is patterned to a periodic strip with a width of about 7 micrometers and a pitch of about 10 micrometers by conventional photolithography method, whereby a first SiO_2 mask **102** is formed (col 7, ln 20-45). Tsuda et al also discloses a GaN crystal film **103** is grown by Metal organic vapor phase epitaxy (MOVPE) to a thickness of about 3 micrometers and a forming a second mask on the GaN film **103**. Tsuda et al also discloses the second mask film **104** is a SiO_2 film with a thickness of about 200 nm with a periodic strip pattern (claim 2 and 7) with a width of about 8 micrometers and a pitch of about 10 micrometers is formed by a photolithography method and forming a GaN single crystal film **105** thereon by MOVPE (col 7, ln 46-67 and col 8, ln 1-30 and Fig 1). Tsuda et al also discloses it is important to select a relationship between the size of each opening of the first mask and the stripe width of the second mask, depending upon required characteristics of a light-emitting device, this reads on applicant's pitch of pattern elements (col 8, ln 31-65). Tsuda et al also discloses a semiconductor substrate including a sapphire substrate can also be used as a substrate, where a sapphire substrate may be peeled off from a semiconductor structure by grinding or etching and the remaining structure can be used as a substrate (claims 20 and 24) (col 22, ln 2-60). Tsuda et al also teaches using SiN_x in place of SiO_2 (col 7, ln 35-45), this reads on applicant's nitride patterns.

Pribat et al or Tsuda et al does not disclose the pitch of pattern elements of one of the plurality of patterns and pitch of pattern elements of another of the plurality of patterns are different from each other.

In a method of checking alignment accuracy in photolithography, Natsume teaches three alignment check patterns **10,20 and 100** are used. Natsume teaches alignment check pattern **10** consists of seven rectangular pattern elements, which are arranged parallel to each other in a row at a constant pitch q. Natsume also teaches alignment check pattern **100** consist of seven rectangular pattern elements which are arranged parallel to each other at a constant pitch p and pitch p differs from the pitch q of the pattern elements of alignment check patterns **10, 20** (col 3, ln 1-50). Natsume also teaches in a composite layout, the underlying check patterns **10, 20** and each of the pattern elements of the overlying pattern **100** partly overlaps both a pattern elements of the first and second check pattern (col 3, ln 51-67). Natsume also teaches the second plurality of patterns partly overlies and partly does not overlie the first plurality of patterns in the direction of the thickness of the crystal (Fig 2(B)). Natsume teaches using different pitches and a region where the patterns do not overlap; therefore overlapping is at least in part due to the difference in pitches because it is a natural effect from using different pitches. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Tsuda et al or Pribat et al's method of forming patterns using photolithography with Natsume's method of checking the alignment in photolithography using pattern elements with different pitches to check the alignment of the patterns (col 2, ln 40-55).

Referring to claim 4, the combination of Tsuda et al and Natsume or the combination of Pribat et al and Natsume does not teach the claimed relationship between the pitch of pattern elements. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Tsuda et al and Natsume or the combination of Pribat et al and Natsume to select any proportion of pitches that would produce a desired alignment

because Natsume does not restrict the ratio of pitches (col 4, ln 40-55). In the absence of unexpected results, any ratio of pitches would have been obvious.

Referring to claims 5-6, the combination of Tsuda et al and Natsume or the combination of Pribat et al and Natsume teaches using patterns with different lengths **13, 14** ('520 Fig 1), which also reads on width because width and length are merely different based on perspective and the width is measure relative to the length, which is not defined.

Referring to claim 7, the combination of Tsuda et al and Natsume or the combination of Pribat et al and Natsume teaches stripes.

Referring to claim 8-9, the combination of Tsuda et al and Natsume or the combination of Pribat et al and Natsume teaches a region where the pattern element **101** does not overlie pattern elements **10,20** in Figure 2(A) of Natsume.

Referring to claim 10-15, the combination of Tsuda et al and Natsume or the combination of Pribat et al and Natsume teaches using SiO_2 mask on a sapphire substrate to grow GaN ('440 col 7, ln 20-67).

Referring to claim 16-19, the combination of Tsuda et al and Natsume or the combination of Pribat et al and Natsume teaches etching and using a masking material. Inherently etching through the dielectric layer will etch a portion of the base layer, this occurs because etch endpoint detection is not perfect and the selectivity is also not perfect. Inherently a nominal portion of the underlying material will be etched.

Referring to claim 20, the combination of Tsuda et al and Natsume or the combination of Pribat et al and Natsume teaches removing the substrate ('440 col 22, ln 10-55).

Referring to claim 23-26, the combination of Tsuda et al and Natsume or the combination of Pribat et al and Natsume teaches using a plurality of patterns with different pitches ('520 col 3, ln 1-67).

4. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuda et al (US 6,294,440) in view of Natsume (US 5,672,520) as applied to claim 1 above, and further in view of Chen et al ("Dislocation reduction in GaN thin films via lateral overgrowth from trenches").

The combination of Tsuda et al and Natsume teach growing GaN films, forming patterns of SiN and growing GaN crystals. The process of forming the patterns in the SiN film requires etching, and since etching inherently will remove a portion of the underlying base layer, which reads on applicant's etching the base layer. However, the combination of Tsuda et al and Natsume does not teach etching to remove more than a nominal amount of the base layer.

In a method of growing GaN, note entire refernence, Chen et al teaches a GaN thin film is grown on a sapphire substrate then trenches are etched into the GaN thin films. Chen et al also teaches covering the trenches with a SiO_2 layer and re-growing a GaN epilayer on the exposed sidewalls of the trench. Chen et al also teaches the additional GaN material re-grown fro mthe sidewalls will have much lower dislocation density. (pg 2062). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Tsuda et al and Natsume by etching trenches into the GaN layer to re-grow GaN from the sidewalls of the trenches, which will have a reduced dislocation density, as taught by Chen et al.

Response to Arguments

5. Applicant's arguments with respect to claims 16-19 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's arguments filed 9/30/2005 have been fully considered but they are not persuasive.

Applicant's argument that the prior art does not teach nitride patterns is noted but is not found persuasive. Pribat and Tsuda both teach masking materials, which are patterned can include SiO_2 or SiN; therefore the prior art does teach using nitride materials. The arguments suggest that the prior art does not teach III-V nitride materials, however interpreted broadly, the claim is open to silicon nitride.

Applicant's arguments regarding claim 4 are noted but are not found persuasive. Tsuda et al teaches patterns with a pitch of 10 μm. Pribat et al does not specify any particular pitch. However, the claimed relationship would appear to cover all possible pitches; therefore does not further limit the invention. A first pitch of 500 μm and a second pitch of 400 μm would result in 2000 μm and would be well within the claimed range. The range is not a significant limitation because semiconductor features are typically on the order of 10 μm, as evidenced by Tsuda et al. Larger features would be obvious, however even features 50 times larger would satisfy the claimed limitation. Virtually any pitch conventionally used in the semiconductor manufacturing art can be used and would satisfy the claimed limitation, absent evidence of unexpected results, the claimed relationship would have been obvious to a person of ordinary skill in the art.

Applicant's arguments regarding claim 10 are noted but are not found persuasive. The prior art clearly shows pattern elements in two direction and regions where the pattern elements overlie and do not overlie, note Fig 2B of Natsume.

Applicant's argument that the prior does not teach etching the base layer is noted but is not found persuasive. Pribat and Tsuda teach patterning and etching to expose a base layer through a patterned layer of SiN. Inherently etching through the SiN layer will etch a portion of the base layer, this occurs because etch endpoint detection is not perfect and the selectivity is also not perfect. Inherently a nominal portion of the underlying material will be etched.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gardner et al (US 6,051,876) teaches a plurality of patterns **152** having different spacing and sizes, which reads on applicants' different pitch, in Figures 1B and 1C.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J. Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Duane Smith can be reached on 571-272-1166. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song
Examiner
Art Unit 1722

MJS
December 9, 2005

ROBERT KUNEMUND
PRIMARY EXAMINER